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| 09/418,031 | 10/14/99 | JANG S | TSMC98-684/6 |

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| EXAMINER | |
|---|---|
| VINH,L | |
| ART UNIT | PAPER NUMBER |
| 1765 | 8 |

DATE MAILED: 05/22/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

| Office Action Summary | Application No. 09/418,031 | Applicant(s) JANG ET AL. | |
|---|---|---|---|
| | Examin r LAN VINH | Art Unit 1765 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc addr ss --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *4/16/2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

**Attachment(s)**

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3, 4* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7, 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al. ( US 6,100,184 ) in view of Hsiao ( US 5,968,842 )

Zhao discloses a method for making a dual damascene interconnect. This method comprises the step of:

forming a substrate having a conductive region (contact region ) 10 ( col 4, lines 14-16 )

forming over the substrate a lower etch stop layer 13 ( silicon oxide ) and an upper dielectric layer 14 ( col 6, lines 33-65 and fig. 2) reads on forming over the substrate a first lower sub-layer and a second upper sub-layer

forming over the lower layer 13 and upper layer 14, an interlevel dielectric ( ILD ) layer 15 ( silicon dioxide ) ( col 6, lines 23-25 )

forming over the IDL layer a photoresist mask pattern 22 to define a subsequent via opening and trench opening over the contact region ( col 7, lines 19-23 and fig. 7 ), utilizing a first plasma etching to etch through the ILD layer 15 and upper layer 14 to the lower layer 13 ( col 7, lines 24-45 and fig. 9 )

employing a second etch method to etch the lower layer 13 from the trench pattern for the interconnect ( col 8, lines 2-5 )

Zhao differs from the instant claimed invention as per claim 1 by using a lower layer 13 ( silicon oxide ) as an etch stop layer instead of a composite etch stop layer.

However, Hsiao discloses a method for reducing dishing in CMP comprises the steps of forming a composite polish stop layer includes two sub-layers ( silicon nitride and oxynitride ) ( col 6, lines 43-46 ). That teaching reads on forming a composite etch stop layer includes two sub-layers.

Hence, one skilled in the art would have found it obvious to combine Zhao's lower etch stop layer and upper dielectric layer to form a composite etch stop layer in view of Hsiao's teaching in order to achieve higher etch selectivity with respect to the conductive region.

Regarding claim 2, fig. 9 of Zhao shows that lower layer 13 prevents the first etching method from etching the contact region.

Regarding claim 3, fig. 10 of Zhao shows that the second etching step removes the lower layer 13 without etching the contact region.

Regarding claim 4, Zhao further discloses the steps of:

forming a barrier metal layer 28 ( TaN ) over the substrate and filling the trench with a conductor material to complete the interconnection structure ( col 8, lines 35-40 )

Regarding claims 5-6, Zhao's method of making a interconnect structure on a semiconductor substrate reads on forming a microelectronics semiconductor layer on a integrated circuit microelectronic fabrication.

Regarding claim 7, Zhao discloses forming the lower layer 13 by CVD ( col 6, lines 3-4)

Regarding claim 9, it is known in the art to fill contact region with tungsten

Regarding claim 10, Zhao discloses that the ILD layer 15 is formed by CVD ( col 6, lines 24-26 )

Regarding claim 11, Zhao discloses filling the trench with copper ( col 8, lines 43-44 )

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al. ( US 6,100,184 ) in view of Hsiao ( US 5,968,842 ) and further in view of Sliwa et al. ( US 5,192,715 )

Zhao as modified by Hsiao has been described above. Zhao and Hsiao differs from the instant claimed invention as per claim 8 by forming a upper dielectric layer of low k dielectric material such as polyimide instead of silicon oxynitride.

However, Sliwa teaches that dielectric layer include polyimide, silicon oxynitride ( col 4, lines 1-3 )

Hence, one skilled in the art would have found it obvious to substitute Zhao's upper layer of polyimide with silicon oxynitride in view of Sliwa's teaching because polyimide and silicon oxynitride are equivalent dielectric material and substitution of one for the other would have been anticipated to produce an expected result.

4. Claim 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al. ( US 6,100,184 ) in view of Hsiao ( US 5,968, 842 ) and further in view of Cronin et al. ( US 5,759,911 )

Zhao discloses a method for making a dual damascene interconnect. This method comprises the step of:

forming a substrate having a aluminum conductive region (contact stud ) 10 ( col 4, lines 14-16 )

forming over the substrate a lower dielectric organic polymer layer 14 ( polyimide ) and a upper dielectric etch stop layer 15 ( col 6, lines 10-25 and fig. 3) reads on forming over the substrate a first lower organic polymer sub-layer and a second upper sub-layer .

forming over the lower layer 14 and upper layer 15, an interlevel dielectric ( ILD ) layer 19 ( silicon dioxide ) ( col 6, lines 61-65 )

forming over the IDL layer a photoresist mask pattern 22 to define a subsequent via opening and trench opening over the contact region ( col 7, lines 19-23 and fig. 7 ), utilizing a first plasma etching to etch through the ILD layer 19 and upper layer 15 to the lower polymer layer 14 ( col 7, lines 25-34 )

removing/stripping the photoresist mask and simultaneously etching the lower polymer layer 14 to complete the interconnection over the aluminum contact region ( col 7, lines 30-45 )

Zhao differs from the instant claimed invention as per claim 12 by using an upper layer 15 ( silicon oxide ) as an etch stop layer instead of a composite etch stop layer and using a contact region of aluminum instead of tungsten.

However, Hsiao discloses a method for reducing dishing in CMP comprises the steps of forming a composite polish stop layer includes two sub-layers ( silicon nitride and oxynitride ) ( col 6, lines 43-46 ). That teaching reads on forming a composite etch stop layer includes two sub-layers.

Hence, one skilled in the art would have found it obvious to combine Zhao's lower layer and upper dielectric etch stop layer to form a composite etch stop layer in view of Hsiao's teaching in order to achieve higher etch selectivity with respect to the conductive region.

Zhao and Hsiao differ from instant claimed invention as per claim 12 by using a contact region of aluminum instead of tungsten.

Cronin teaches that aluminum or tungsten can be used to fill contact region or stud connection in a semiconductor structure ( col 10, lines 3-5 )

Hence, one skilled in the art would have found it obvious to substitute Zhao and Hsiao aluminum contact stud with tungsten stud in view of Cronin's teaching because aluminum and tungsten are equivalent conductive material and substitution of one for the other would have been anticipated to produce an expected result.

Regarding claim 14, Zhao discloses forming a barrier metal layer 28 ( TaN ) over the substrate and filling the trench with a conductor material to complete the interconnection structure ( col 8, lines 35-40 )

Regarding claim 16, Zhao discloses that lower polymer layer comprises of low dielectric constant spin-on-polymer such as polyimide ( col 6, lines 15-17 )

Regarding claim 17, Zhao discloses that upper layer 15 ( silicon dioxide ) is formed by CVD ( col 6, lines 24-26 )

Regarding claim 19, Zhao discloses filling the trench with aluminum or copper ( col 8, lines 43-44 )

### *Response to Arguments*

5. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAN VINH whose telephone number is 703 305-6302. The examiner can normally be reached on Monday-Friday 8:30 -6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BENJAMIN L UTECH can be reached on 703 308-3836.

ROBERT KUNEMUND
PRIMARY EXAMINER

LV
May 16, 2001